In the Claims:

1. (Currently Amended) A method of performing configuration or control of a hardware-based subsystem that includes multiple hardware registers that define multiple configurations of the hardware-based subsystem and that are connected to a processor via a system bus, the method comprising:

providing together with the subsystem a configuration/control unit having a controller portion and a read-only storage portion storing multiple sets of configuration data, each of the sets of configuration data including configuration parameters for each of the multiple registers, and each of the sets of configuration data defining a respective one of the multiple configurations; and

the configuration/control unit, in response to a single register write that identifies one of the sets of configuration data, encapsulating the multiple hardware registers by performing configuration, reconfiguration, initialization or control of the subsystem, and by including storing writing, the configuration parameters of the identified set of configuration data, [[in]] from the read-only storage portion to each of the multiple registers of the hardware subsystem.

2. (Currently Amended) The method of claim 1, wherein the subsystem is a universal serial bus (USB) block, and the multiple configurations include Control mode, Interrupt mode, Isochronous mode, and Bulk mode, each of the modes encapsulated by a single write to a common register location, and wherein ~~the subsystem is a hardware subsystem, and~~ the configuration/control unit is a hardware configuration/control unit.

3. (Previously presented) The method of claim 2, wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit.

4. (Currently Amended) The method of claim 1, wherein the ~~storing~~ writing of the configuration parameters of the identified set in the multiple registers is implemented

using a bus having a width sufficient to simultaneously store the configuration parameters of the identified set.

5. (Previously presented) The method of claim 1, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data.

6. (Currently Amended) A hardware-based subsystem having self-configuration capabilities and a processor connected to a system bus, comprising:

a hardware register section that is connected to the system bus and including multiple hardware registers that define multiple configurations of the hardware subsystem; and

a configuration/control unit having a controller portion and a read-only storage portion storing multiple sets of configuration data, each of the sets of configuration data including configuration parameters for each of the multiple registers, and each of the sets of configuration data defining a respective one of the multiple configurations; wherein the configuration/control unit is configured, responsive to a single register write that identifies one of the sets of configuration data, to encapsulate the multiple hardware registers by performing configuration, reconfiguration, initialization or control of the subsystem, including storing the configuration parameters of the identified set in the multiple hardware registers of the subsystem.

7. (Currently Amended) The subsystem of claim 6, wherein the subsystem is a universal serial bus (USB) block, and the multiple configurations include Control mode, Interrupt mode, Isochronous mode, and Bulk mode, each of the modes encapsulated by a single write to a common register location, and wherein ~~subsystem is a hardware subsystem, and~~ the configuration/control unit is a hardware configuration/control unit.

8. (Previously presented) The subsystem of claim 7 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit.

9. (Previously presented) The subsystem of claim 6, further comprising a bus having a width sufficient to simultaneously store the configuration parameters of the identified set in the multiple registers.

10 (Previously presented) The subsystem of claim 6, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data.

11. (Currently Amended) For use in a system that includes a processor coupled to a hardware subsystem via a system bus, the hardware subsystem including a configuration/control unit and a plurality of hardware registers that define multiple configurations of the subsystem, a method of configuring the subsystem comprising:

storing a plurality of sets of configuration data in a read-only memory of the configuration/control unit, each of the sets of configuration data including configuration parameters for each of the plurality of registers, and each of the sets of configuration data defining a respective one of the multiple configurations; and

responsive to the configuration/control unit receiving, from the processor, a single register write that identifies one of the sets of configuration data, encapsulating the plurality of registers by writing the configuration parameters of the identified set from the read-only memory to the plurality of registers wherein the encapsulating includes configuration, reconfiguration, initialization or control of the hardware subsystem.

12. (Previously presented) The method of claim 11, wherein the configuration/control unit is a state machine.

13. (Previously presented) The method of claim 11, wherein the subsystem is a USB block comprising a plurality of ports that can operate in different modes responsive to which of the sets of configuration data is written to the plurality of registers.

14. (Previously presented) The method of claim 11, wherein the storing of the configuration parameters of the identified set in the plurality of registers is implemented using a bus having a width sufficient to simultaneously store the configuration parameters of the identified set.

15. (Previously presented) The method of claim 11, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data.